Remarks

In the non-final Office Action mailed on 8 January 2008, the Examiner has rejected all the remaining claims 1, 3-7, 9-13, and 15-16 under 35 U.S.C. §103(a) as being obvious in view of the combination of U.S. Patent No. 5,357,572 (Bianco) and U.S. Patent No. 5,278,903 (Matsui). Applicants respectfully traverse the rejection and request reconsideration and withdrawal of same.

35 U.S.C. §103 Rejection

The Examiner has rejected the pending claims as obvious over Bianco in view of Matsui. Regarding claim 1, the Examiner has suggested that Bianco teaches essentially all the claim limitations of pending claim 1. The Examiner has further suggested that Matsui teaches deleting secure information when a scan signal is detected, and that the motivation to combine Bianco with Matsui is to protect sensitive information from being viewed/detected during a scan test signal. Applicants respectfully disagree.

Applicants submit that regardless of what Bianco does teach, it does not teach clearing secure information within an integrated circuit. The Examiner has suggested that Bianco does teach such a feature (Office Action page 3). Applicants have previously discussed this issue and the Examiner has withdrawn the previous 102 rejection. Regardless, the Examiner has supplied Matsui, suggesting Matsui alleviates this weakness of Bianco. Applicants maintain that neither Bianco nor Matsui, nor the combination of Bianco and Matsui, teaches the recited erasure. Applicants further submit that the Examiner has improperly combined Matsui with Bianco to alleviate this weakness, and that Matsui is not analogous art.

MPEP 2141.01(a) recites: "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." Applicants submit that Matsui is neither in the field of Applicants' endeavor, nor reasonably pertinent to the particular problem with which the Applicants were concerned. The pending application is within the field of integrated circuit testing. Specifically, the application pertains to boundary scan issues relating to securing data within an integrated circuit. Matsui teaches a

document information imaging system. Specifically, Matsui pertains to scanning documents into a scanner to digitize images of the documents for information processing. One skilled in the art of integrated circuit design would not consider the art of document image processing to solve problems relating to erasing secure information within an integrated circuit.

MPEP 2143.02 recites: "The prior art can be modified or combined to reject claims as *prima facie* obvious as long as there is a reasonable expectation of success." Bianco relates to the art of integrated circuit design, and specifically, relates to disabling access to secure information in an integrated circuit by disabling enable signals which control access to the secure information. Matsui relates to the art of processing information from paper documents using a scanner. Applicants submit that there is no reasonable expectation of success for combining Matsui with Bianco. The Examiner has relied upon Matsui as exemplary of erasing information, but the reference is so far afield from the claimed invention or from Bianco that Matsui's teaching of erasure is simply inapplicable to Bianco or the claimed invention. To suggest otherwise is to suggest that anything or any teaching that "erases" something could be combined with Bianco. For example, a rubber eraser on a pencil, a chalkboard eraser, or a magnet used to erase a hard drive containing secure data. Although a magnet may "erase" digital data stored magnetically, it cannot be expected to erase data in Bianco. In like manner, although Matsui teaches "erasing" a portion of a scanned document image, there is no basis for combining it with Bianco because there is no reasonable expectation of success.

Although the Examiner has indicated with her withdrawal of the 102 rejection and the inclusion of the Matsui reference that Bianco fails to teach the recited erasing limitation, the Examiner seems to equivocate on her position as to whether Bianco alone teaches all the recited elements. In particular, the Examiner states on page 3 of her office action: "Even though Bianco et al.'s address erasure is specifically to erase sensitive subcircuites, as one ordinary skill in the can understands, the office herein provided Matsui et al. reference that discloses identification information delete unit deleting identification information when a read scan signal is detected (see col. 3 lines 54-61)." Thus it appears that the Examiner continues to assert that Bianco alone teaches all the elements of the rejected claims.

In view of this ambiguity, Applicants feel it would be appropriate to clarify again that Bianco does not teach the limitation of claim 1 recited herein: "a reset generator to clear all secure information within the integrated circuit." The Examiner has specifically cited sections column 6, lines 19-31, column 5 lines 19-36, and column 4 lines 7-28 claiming that the claim 1 limitation is taught. Column 6 lines 19-31 specifically recites (emphasis added):

> In this case the set scan control 14d includes an electrically erasable or ultraviolet **erasable PROM (EE-PROM or UV-PROM) 36 that includes an address for each sensitive subcircuit**. A program signal is applied at program input 18 that includes a sequential bit sequence to enable or inhibit each sensitive subcircuit address in the EE-PROM 36. The contents of the EE-PROM 36 are decoded by a decoder 38 and applied to respective AND gates 40a, 40b, 40c, 40d for each of the sensitive subcircuits **to control the access of a set/scan enable signal** at input 20 to the multiplexers for these subcircuits; the set/scan enable 20 is connected to the second inputs for each of the AND gates.

Referring to FIG. 5 in Bianco, Applicants submit that erasing EE-PROM 36 is not operable to "clear all secure information within the integrated circuit" as recited in rejected claim 1. Erasing EE-PROM 36 in Bianco only disables enable lines 40a-d. The secure information inside the IC is not cleared.

The Examiner has further cited column 5 lines 19-36 in Bianco, which recites (emphasis added):

> ...14a cannot be changed back to the enabling state by a copyist once it has been placed in a disabling state. While various types of fuses or irreversible switches could be used for this purpose, a fusible-link PROM cell is a convenient way to implement the latch-out in a monolithic IC. Once the programming input 18 is made active, the **PROM cell 22 is erased and permanently prevents the set/scan enable signal at input 20 from reaching the sensitive subcircuits**. Other control elements that can be reprogrammed from a disabling back to an enabling state and then erased again to allow post-manufacturing set/scan testing of the sensitive subcircuits, such as electrically or ultraviolet erasable...

Referring to FIG. 2 in Bianco, Applicants submit that erasing PROM 22 is not operable to "clear all secure information within the integrated circuit" as recited in claim 1. Bianco makes clear that his "sensitive subcircuits" are not erased. Rather, his PROM 22 is erased. Erasing

PROM 22 in Bianco only disables enable line 16S. The secure information inside the IC is not cleared.

The Examiner has further cited Column 4 lines 7-28 in Bianco, which recites (emphasis added):

> In accordance with the invention, a special set/scan control circuit 14 is provided to inhibit set/scan access to the sensitive subcircuits, while permitting set/scan access to the other subcircuits. The set/scan control circuit 14 generates two separate set/scan enable signals, one over line 16S for the sensitive subcircuits and the over line 16N for the non-sensitive subcircuits, as determined by an external programming input 18. A second input 20 is provided to the set/scan control circuit 14 to set the circuit to an enabled state when set/scan testing is desired. When the programming input 18 is inactive and a set/scan enable signal is applied to input 20, both of the output lines 16S and 16N are enabled, allowing both the sensitive and non-sensitive circuits to be included in the set/scan test chain. Once the program input 18 has been activated, only the non-sensitive subcircuits can be set to known values and read back out in a set/scan test mode; **the sensitive subcircuits are bypassed and thus cannot be set to known values or read out of the device**. A copyist is thereby denied access to the sensitive subcircuits and prevented from determining their functions or designs.

Referring to FIG. 2 in Bianco, Applicants submit that disabling line 16N is not operable to "clear all secure information within the integrated circuit" as recited in claim 1. Disabling line 16N in Bianco only bypasses sensitive subcircuit 2S. The secure information inside sensitive subcircuit 2S is not cleared.

Applicants submit that disabling access to secure information within an integrated circuit is substantially different than clearing secure information within an integrated circuit. When secure information remains within the integrated circuit, it is possible to restore functionality necessary to retrieve the secure data. This could be accomplished by gaining access to the internal logic of the integrated circuit and restoring the functionality of the disabled select logic for the secure information. When secure information within an integrated circuit is cleared, the information would not be available for restoration in this previously described manner or in any manner. This is a substantial difference between Bianco and the claimed invention.

Because Bianco does not teach clearing secure information within an integrated circuit, and Matsui is not properly combined and is non-analogous art, no prior art of record teaches or

reasonably suggests the limitations in the pending claims. For at least the reasons provided above, Applicants submit that independent claims 1, 7, and 13, and dependent claims 3-6, 9, and 15-16 are non-obvious over the cited prior art, and thus, respectfully request withdrawal of the outstanding rejection and allowance of the pending claims.

Conclusion

Applicants have thoroughly discussed and traversed the Examiners rejection of all claims under §103 and have requested reconsideration and withdrawal of all rejections.

No additional fees are believed due. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,

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